

April 1, 2003  
Case No. PHB 34,365 (7790/234)  
Serial No.: 09/964,154  
Filed: July 11, 2000  
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**REMARKS**

In the Non-Final Office Action, Examiner Shapiro rejected pending claims 1-8 on various grounds. The Applicants respond to each rejection as subsequently recited herein, and respectfully requests reconsideration and further examination of the present application under 37 CFR § 1.112:

A. Claims 1-5 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No., 6,384,806B1 to *Matsueda* et al.

The Applicant has thoroughly considered Examiner Choi's remarks concerning the patentability of claims 1-5 over *Matsueda*. The Applicant has also thoroughly read *Matsueda*. As illustrated in FIG. 17 of *Matsueda*, the Applicant respectfully asserts that *Matsueda* discloses signal bus lines D1T-DUT and D1B-DuB, but fails to disclose teach or suggest the signal processing circuits feeding signal bus lines D1T-DUT and D1B-DuB to circuits 101A and 101B. Thus, *Matsueda* fails to disclose, teach or suggest "respective signal processing circuits connected to each bus line", and "the signal processing circuits associated with the bus lines are integrated as respective circuit blocks on the device substrate with the individual signal processing circuit blocks associated with adjacent column conductors being located close together on the device substrate" as recited in independent claim 1.

To better differentiate the present invention of *Matsueda* and the remaining art of record, the Applicant has cancelled claims 1-8 herein and added claims 9-12. The Applicant respectfully asserts that *Matsueda* and the remaining art of record, in combination, fail to disclose, teach or suggest "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein each individual signal processing circuit associated with a first address conductor of a first group and a last address conductor of a second group are adjacent on said substrate" as recited in independent claim 9. Withdrawal of the rejection of claims 1-5 under §102(e) as being anticipated by *Matsueda* and allowance of claims 9-12 is therefore respectfully requested.

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B. Claim 6 was rejected under 35 U.S.C. §103(a) as being anticipated by U.S. Patent No., 6,384,806B1 to *Matsueda* et al. in view of U.S. Patent No. 5,751,279 to *Okumura* et al.

The Applicant has cancelled claim 6 herein without disclaimer or prejudice as to the claimed subject matter. Withdrawal of the rejection of claim 6 under §103(b) as being unpatentable over *Matsueda* in view of *Okumura* is therefore respectfully requested.

C. Claims 7 and 8 were rejected under 35 U.S.C. §103(a) as being anticipated by U.S. Patent No., 6,384,806B1 to *Matsueda* et al. in view of U.S. Patent No. 6,255,705B1 to *Zhang* et al.

The Applicant has cancelled claims 7 and 8 herein without disclaimer or prejudice as to the claimed subject matter. Withdrawal of the rejection of claims 7 and 8 under §103(b) as being unpatentable over *Matsueda* in view of *Zhang* is therefore respectfully requested.

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**SUMMARY**

Examiner Shapiro's §§102(b) and 103(a) rejections of claims 1-8 have been obviated by the cancellation of claims 1-8. The Applicant has supported the patentability of new claims 9-12 over the art of record. The Applicant respectfully submits that claims 9-12 as added herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, Examiner Shapiro is respectfully requested to contact the undersigned at the telephone number listed below.

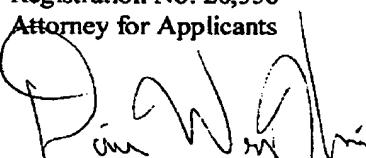
Dated: April 1, 2003

Respectfully submitted,  
MARTIN J. EDWARDS

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